

a first interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor;

a first interconnection layer formed on the first interlevel dielectric film; and

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D1
cont. a memory cell composed of the ferroelectric capacitor and the memory cell transistor, wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode;

wherein the memory cell comprises a memory cell array arranged in a matrix, wherein the first interconnection layer extends only in one direction with respect to the top and bottom electrodes, and

wherein a plurality of the top electrode is arranged only in a row with respect to the direction of the length of the bottom electrode.

6. (Amended) The device of Claim 1, wherein the first interconnection layer includes:

D2 a storage line connected to the top electrode of the ferroelectric capacitor and to the first doped layer of the memory cell transistor, the storage line having a linear planar pattern; and the bit line connected to the second doped layer of the memory cell transistor, and wherein the bit line does not overlap with the top electrode in the planar layout.

8. (Twice Amended) The device of Claim 1 further comprising:

D3 a second interlevel dielectric film formed to cover the first interconnection layer, wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode.